Scientific Report

on the implementation of the project PN-III-P4-ID-PCE-2016-0122, entitled *Nanostructures for quantum and plasmonic computing* in the period January – December 2018

In the 2018 stage of the project, we focused on the activities

Act. 2.1 – Development of a ballistic configuration for quantum circuits using edge states,

Act. 2.2 – Investigation of new configurations for quantum computing using spins in nanostructures with gate-tunable Rashba spin-orbit coupling,

Act. 2.3 – Development of a correspondence between implemenations of qubits with spins and valley states, and

Act. 2.4 – Investigation of new configurations for quantum computing using valley states; this activity will be continued in 2019 as Act 3.1.

The obtained results are detailed in the following.

Development of a ballistic configuration for quantum circuit implementation using edge states

Presently, there are two ways to implement quantum logic circuits: using nanostructures that manipulate localized quantum states of spins [1], charge [2] or superconducting [3], or configurations based on the quantum interference in nanosystems with ballistic (collisionless) transport. The last way of implementing quantum logic gates, which includes the interference between edge states in interferometers defined by quantum point contacts (QPCs) [4] realized in two-dimensional electron gases (2DEGs), has the advantage of a good sensitivity [5] and possibility of modelling analytically the propagation of electronic wavefunction. Therefore, we have focused on finding a compact and reconfigurable configuration for implementing logic gates using edge states.

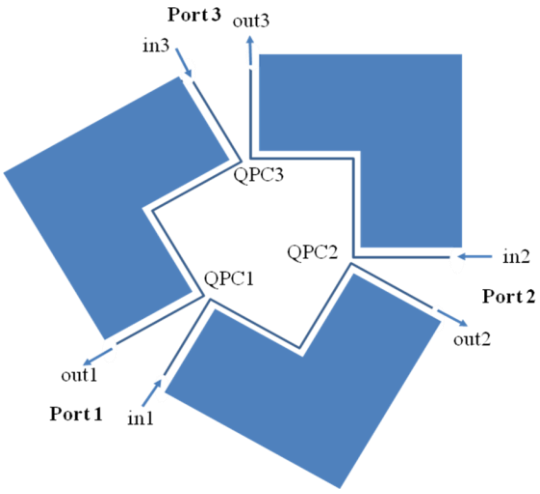


Fig. 1

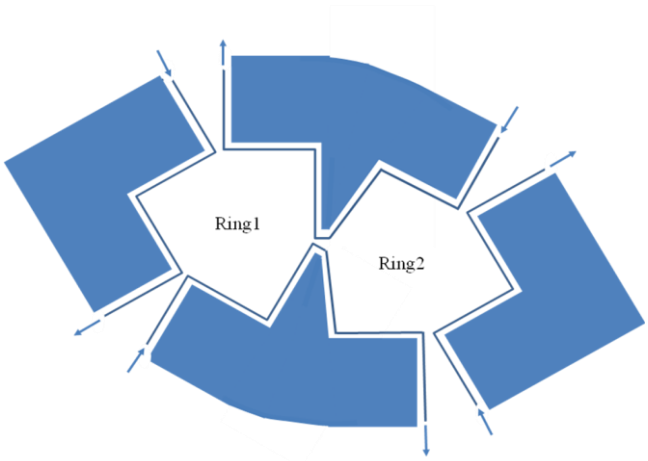


Fig. 2

The proposed configuration, represented in Fig. 1, consists of a 3-port interferometer working in the integer Hall effect regime in a 2DEG, the charge carriers propagating along the edge

states/channels. Two such nterferometers can be combined in order to realize complex logic circuits, as suggested in Fig. 2. The input logic states are encoded in the potentials applied on the thee QPCs that define the interferometer, the output logic states being determined by the transmission coefficient at each gate. As will be shown in the following, this configuration allows the implementation of different logic gates at different ports, and so the possibility of processing in parallel of different quantum algorithms.

Assuming a spin-independent scattering at each potential barrier induced by QPCs, and a uniform magnetic field *B* applied along *z*, perpendicular to the (*x*,*y*) plane of the 2DEG, such that the vector potential is $A=(0,Bx,0)$, the single-particle Hamiltonian of an electron with effective mass *m* and wavevector components along *x* and *y* directions denoted as k_x and, respectively, k_y, is [4]

$$H=\frac{\omega_d^2}{\omega_t^2}\frac{\hbar^2k_y^2}{2m}+\frac{\hbar^2k_x^2}{2m}+\frac{m\omega_t^2}{2}(x-x_0)^2 \tag{1}$$

where ω_d is the frequency associated to the transverse confinement along *x*, $\omega_t=\sqrt{\omega_d^2+\omega_c^2}$ with $\omega_c=eB/m$ the cyclotronic frequency, and $x_0=\hbar k_y\omega_c/(\omega_t^2m)$.

The dispersion relation of the discrete energy levels is

$$E_{n,k_y}=\hbar^2k_y^2\frac{\omega_d^2}{2m\omega_t^2}+\hbar\omega_t\left(n+\frac{1}{2}\right), \tag{2}$$

the two edge states, located on opposite edges $\pm x_0$, and correspunding to wavevector components $\pm k_y$, propagating at the same (fixed) energy value. We assume that *n* = 0, such that only the fundamental energy level is occupied, i.e. *E* takes values between $\hbar\omega_t/2$ and $3\hbar\omega_t/2$. In a 2DEG the energy of charge carriers (the Fermi level) can be controlled by applying a gate voltage [6].

The action of each QPCs, situated at $x=x_i$, i = 1,2,3, and assumed to separato regiuns in which the electron has the same wavevector *k*, is modelled by a potential $U_i(x_i)=(\hbar^2/2m)\gamma_i\delta(x_i)$, the reflexion and transmission coefficients of the QPC depending on the applied potential U_i as: $r_i=\gamma_i/(2ik-\gamma_i)$, and, respectively, $t_i=2ik/(2ik-\gamma_i)$.

Under these circumstances, the output vector of the 3-port interferometer, $out^T=(out1,out2,out3)$, depends linearly on the input vector $in^T=(in1,in2,in3)$, which describes the amplitudes of the input wavefunctions at the three ports:

$$\begin{pmatrix}out1\\out2\\out3\end{pmatrix}=\begin{pmatrix}M_{11}&M_{12}&M_{13}\\M_{21}&M_{22}&M_{23}\\M_{31}&M_{32}&M_{33}\end{pmatrix}\begin{pmatrix}in1\\in2\\in3\end{pmatrix} \tag{3}$$

the elements of the matrix *M* being given by

$$M_{11} = r_1 + \frac{t_1^2 r_2 r_3 \exp(i\Phi)}{\Delta},\ M_{21} = \frac{t_1 t_2 \exp(i\phi_{12})}{\Delta},\ M_{31} = \frac{t_1 r_2 t_3 \exp[i(\phi_{12}+\phi_{23})]}{\Delta} \quad (5a)$$

$$M_{12} = \frac{t_2 r_3 t_1 \exp[i(\phi_{23}+\phi_{31})]}{\Delta},\ M_{22} = r_2 + \frac{t_2^2 r_3 r_1 \exp(i\Phi)}{\Delta},\ M_{32} = \frac{t_2 t_3 \exp(i\phi_{23})}{\Delta} \quad (5b)$$

$$M_{13} = \frac{t_3 t_1 \exp(i\phi_{31})}{\Delta},\ M_{23} = \frac{t_3 r_1 t_2 \exp[i(\phi_{31}+\phi_{12})]}{\Delta},\ M_{33} = r_3 + \frac{t_3^2 r_1 r_2 \exp(i\Phi)}{\Delta} \quad (5c)$$

where $\phi_{ij} = kL_{ij}$ are the phases acquired at propagation from port *i* to port *j*, separated by the distance L_{ij}, $\Phi = \phi_{12} + \phi_{23} + \phi_{31}$, and $\Delta = 1 - r_1 r_2 r_3 \exp(i\Phi)$. The transmission coefficient at port *i* is the square of the modulus of *outi*, *i* = 1, 2, 3. We associate to this transmission coefficient *T* the output logic value 1 if $T > T_{th}$, where T_{th} is a threshold value, and the output logic value 0 if $T < T_{th}$. Similarly, we encode the input logic values in the potentials appliced on the three QPC, (U_1, U_2, U_3), such that each U_i, *i* = 1, 2, 3 has logic value 0 if equal to $V_0 = 0$ or logic value 1 if equal to $V_1 = 0.5$ eV.

For exemplification, in Figs. 3(a), 3(b) and 3(c) we illustrate the energy dependencies of the 3 ports: 1, 2 and respectively 3, if $in^T = (1,1,0)$, the input logic states encoded as (U_1, U_2, U_3) being specified in the legend. In this case, the transmission coefficient maxima at each port can be higher than 1 (but smaller than 2), since there are two inputs, each with amplitude 1. We used in simulations $m = 0.067 m_0$, with m_0 the free electron mass (as in the 2DEG system GaAs/AlAs), $\hbar\omega_d = \hbar\omega_c =$ 4 meV, and $L_{12} = L_{23} = L_{31} =$ 100 nm. The three-dimensional representations on the right of Figs. 3(a)-(c) show the same dependencies, emphasizing the overlapping curves.

As can be observed from these figures, the transmission coefficients at all ports vary continuously with energy, except for the input logic state (111), for which it has abrupt variations at resonant energies, E_r. Depending on the values of energy *E*, the chosen threshold values and the potentials applied on the QPC, Figs. 3(a)-(c) suggest that at each port one can implement the following operations/logic gates:

I. For *out*1,

i) at resonant energies E_r, for T_{th} = 0.5, we can implement:

a) the logic gate OR for U_1 and U_2, if U_3 = 0
b) the logic gate NAND for U_1 and U_3, if U_2 = 1
c) the logic gate NAND for U_2 and U_3, if U_1 = 1
d) the logic gate Set 1 (sets the output logic gate as 1), if (U_2,U_3) = (01) or (10)

ii) outside resonance, for T_{th} = 0.3, we can implement:

a) the logic gate OR for U_1 and U_3, irrespective of U_2
b) the logic gate Set 1, if U_1 = 1 or U_3 = 1

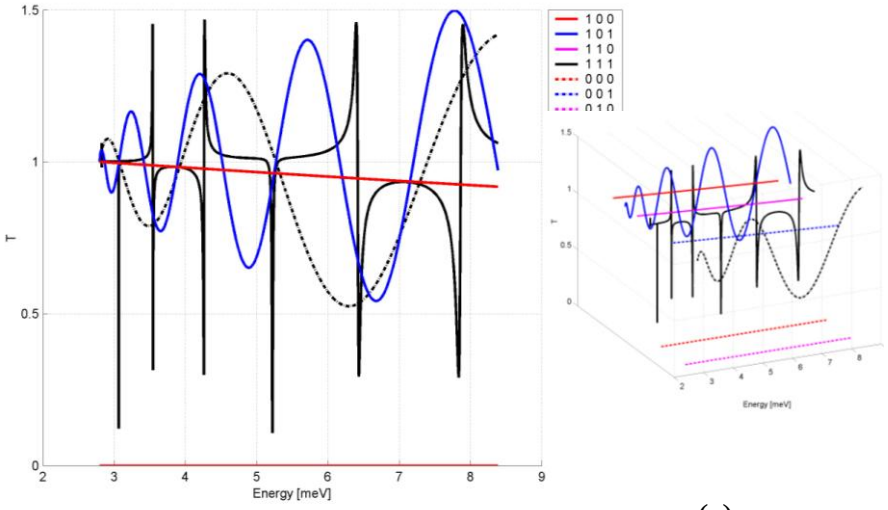
iii) at $E \cong$ 4.3 meV, for T_{th} = 1.2, we can implement:

a) the logic gate Erase (sets the output logic gate as 0) for U_1 = 1, irrespective of U_2 and U_3
b) the logic gate AND for U_2 and U_3, if U_1 = 0

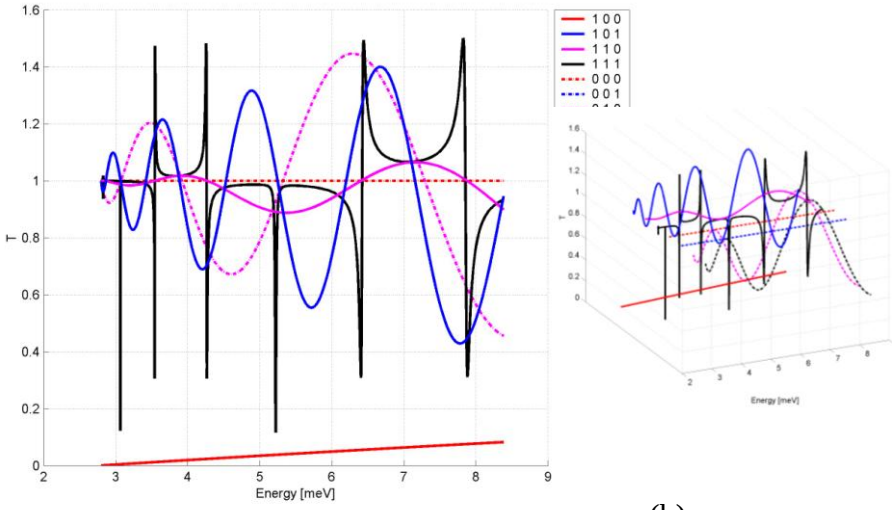
iv) at $E \cong$ 5.7 meV, for T_{th} = 1.25, we can implement:

a) the logic gate Erase if (U_1,U_2) = (00), (01) or (11), irrespective of U_3

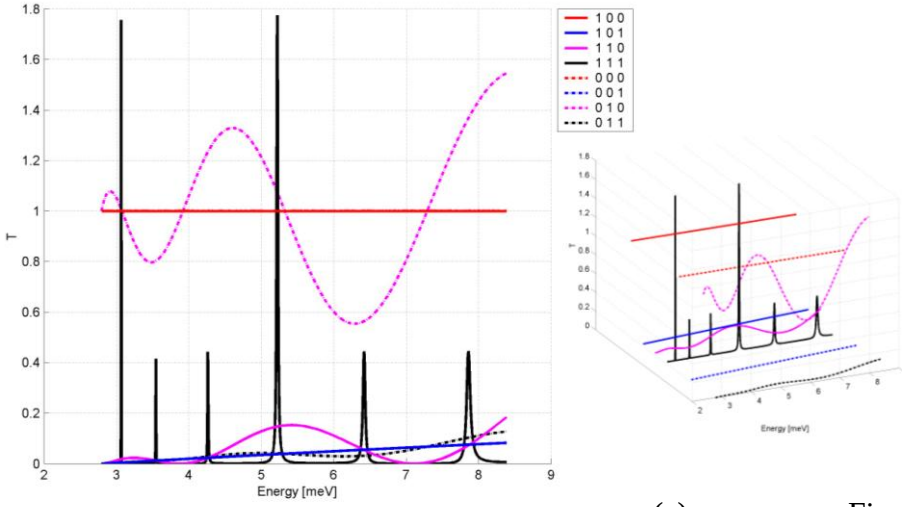
b) the logic gate AND for U_1 and U_3, if $U_2 = 0$



(a)



(b)



(c) Fig. 3

v) at $E \cong 6$ meV, for $T_{th} = 0.7$, we can implement:

a) the logic gate NOR for U_1 and U_3, if $U_2 = 0$

b) the logic gate Set 1 if $U_1 = 1$, irrespective of U_2 and U_3

c) the logic gate Identity for U_1, if (U_2,U_3) = (00), (10), or (11)

vi) at $E \cong$ 7.7 meV, for T_{th} = 1.2, we can implement:

a) the logic gate Erase if U_3 = 0, irrespective of U_1 and U_2
b) the logic gate AND for U_1 and U_3, if U_2 = 0
c) the logic gate AND for U_2 and U_3, if U_1 = 0
d) the logic gate CNOT if U_3 = 1, with U_1 the target bit and U_2 the control bit

II. For *out*2,

i) at resonant energies E_r, for T_{th} = 0.5, we can implement:

a) the logic gate NOR for U_1 and U_2, if U_3 = 1
b) the logic gate NOR for U_1 and U_3, if U_2 = 1
c) the logic gate CNOT if U_1 = 1, with U_2 target bit and U_3 control bit
d) the logic gate Set 1, if U_1 = 0, irrespective of U_2 and U_3
e) the logic gate NOT for U_1, if (U_2,U_3) = (00) or (11)

ii) outside resonance, for T_{th} = 0.3, we can implement:

a) the logic gate OR for U_2 and U_3, if U_1 = 0
b) the logic gate Set 1, if U_1 = 0, U_2 = 1 or U_3 = 1

iii) at $E \cong$ 4.8 meV, for T_{th} = 1.2, we can implement:

a) the logic gate Erase if U_1 = 0, U_2 = 1 or U_3 = 0
b) the logic gate AND for U_1 and U_3, if U_2 = 0

iv) at $E \cong$ 5.7 meV, for T_{th} = 0.8, we can implement:

a) the logic gate Set 1 if U_1 = 0 or U_2 = 1

v) at $E \cong$ 6 meV, for T_{th} = 1.2, we can implement:

a) the logic gate Erase if U_1 = 1 or U_2 = 0
b) the logic gate NOT for U_1, if (U_2,U_3) = (10) or (11)

III. For *out*3,

i) outside resonance, for T_{th} = 0.5, we can implement:

a) the logic gate NOR for U_2 and U_3, if U_1 = 1
b) the logic gate NOT for U_3, if (U_1,U_2) = (00), (01) or (10)

ii) outside resonance, at $E \cong$ 5-7 meV, for T_{th} = 0.8, we can implement:

a) the logic gate NOR for U_2 and U_3, irrespective of U_1

iii) outside resonance, at $E \cong$ 4-5.2 meV, for T_{th} = 0.8, we can implement:

a) the logic gate NOR for U_1 and U_3, if U_2 = 1
b) the logic gate NOR for U_2 and U_3, if U_1 = 1
c) the logic gate NAND for U_1 and U_2, if U_3 = 0
d) the logic gate NOT for U_3, if (U_1,U_2) = (00) or (10)
e) the logic gate Erase if U_3 = 1, irrespective of U_1 or U_2

iv) at resonance, $E \cong$ 5.2 meV, for T_{th} = 0.8, we can implement:

a) the logic gate modified CNOT (modifies the target bit value if the control bit is 0) if U_1 = 1, with U_3 target bit and U_2 control bit

Because the wavefunctions can be detected at each outputs/ports, the examples above suggest that one can implement at each port a large number of logic gates at determined energies (via gae voltages) and threshold values for the transmission coefficient/measured current. Similar results are obtained for $in^T = (1,0,0)$ and $in^T = (1,1,1)$.

Besides offering the possibility to process in parallel different quantum gates/algorithms at different outputs for the same input logic states, the 3-port configuration in Fig. 1 can be combined with another similar one (see Fig. 2), such that the first interferometer (with ports 1, 2 and 3) is conditioned by the output of the second one (with ports 1', 2' and 3'). In addition, the logic gate implemented at ports 1 or 3 is restricted/selected among the possible implementations (see the examples above) by the fact that QPC2 is identical to cu QPC2'.

The simulation results fo this 3-port interferometric configuration that uses edge states are submitted to an ISI journal (see **A1**).

Investigation of new configurations for quantum computing using spins in nanostructures with gate-controlled Rashba spin-orbit coupling

We have studied two configurations, both implemented in a 2DEG with gate-controlled Rashba spin-orbit coupling, in which charge carriers propagate in the ballistic regime. In these configurations the qubit is coded in spin states, allegedly robust, and is manipulated via the Rashba spin-orbit interaction.

The first configuration, represented in Fig. 4, consists of two incoming quantum wires, *a* and *b*, cupled via the Rashba interaction in the region Ω_0, which modulates the functionality of the system, allowing the implementation of logic gates such as OR, AND XOR or CNOT. The outgoing quantum wires are denited *c* and *d*. The coupling region, with a tuneable Rashba coefficient α, contains a QPC, formed from two barriers of height V_0 and areas $\Delta y_1 \times w$ and $\Delta y_2 \times w$, which can be symmetric or asymmetric. The interface between the coupling region and the Ω_s regions in which the quantum wires are separated is denoted by Γ_s and has an area $L_x \times L_y$.

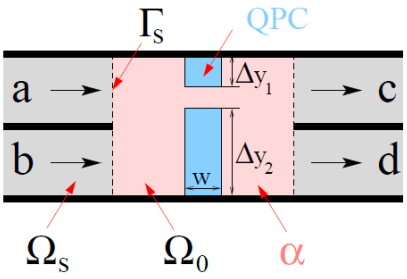


Fig. 4

The ballistic transport in this system is modelled by the R-matrix model [7, 8]. For the system in Fig. 4we define four input logic states $S = A, B, C, D$ as:

$$A = \frac{1}{\sqrt{2}}|\uparrow\rangle_a + \frac{1}{\sqrt{2}}|\uparrow\rangle_b,\ B = \frac{1}{\sqrt{2}}|\uparrow\rangle_a + \frac{1}{\sqrt{2}}|\downarrow\rangle_b, \quad (6a)$$

$$C = \frac{1}{\sqrt{2}}|\downarrow\rangle_a + \frac{1}{\sqrt{2}}|\uparrow\rangle_b,\ D = \frac{1}{\sqrt{2}}|\downarrow\rangle_a + \frac{1}{\sqrt{2}}|\downarrow\rangle_b \quad (6b)$$

corresponding to (*a*,*b*): (0,0), (0,1), (1,0), (1,1). The electrons prepared in one of the *S* states by a coherent superposition of the wavefunctions in the input quantum wires *a* and *b* interfere

in teh coupling region, so that in the outgoing wires $s = c, d$ we obtain spin-polarized currents, with the polarization,

$$p_s^S = (T_{s\uparrow}^S - T_{s\downarrow}^S)/(T_{s\uparrow}^S + T_{s\downarrow}^S) \quad (7)$$

where $T_{s\uparrow,\downarrow}^S$ denotes the transmission coefficient from state S to state s for electrons with spins up and down, respectively, and the logic values of output states is defined in terms of the polarization sign.

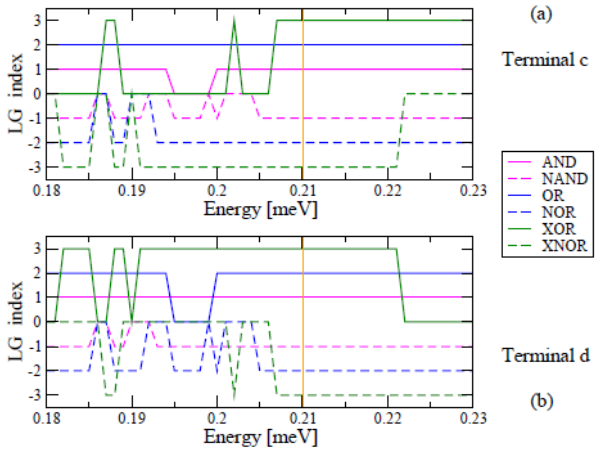


Fig. 5

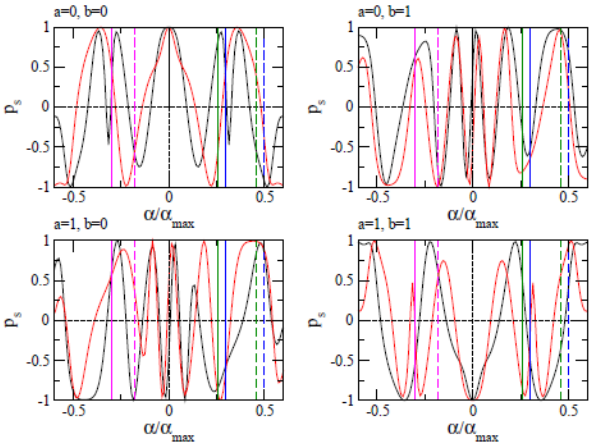


Fig. 6

To exemplify the working of the system in Fig. 4, we assume that the sign of polarization can be determined unambiguously for a net spin current higher than 10%, and define an LG index of realization of the given logic gate as +1 for AND, -1 for NAND, +2 for OR, -2 for NOR, +3 for XOR, -3 for XNOR and +4 for CNOT. The objective is to establish, for electrons with a certain energy if, by varying the Rashba coefficient in the interval $[-\alpha_{max}, \alpha_{max}]$, with α_{max} = 20 meV nm, we can implement these gates. If we can do this, the LG index takes the indicated value, otherwise LG = 0. The energy dependence of LG for a symmetric QPC with $\Delta y_1 = \Delta y_2 = L_y/4$, $w = L_x/8$, fabricated in an InAs 2DEG, with $m = 0.023m_0$, L_x = 4 μm, L_y = 1 μm, and V_0 = 1 eV, is presented in Fig. 5(a) for spin current measurements in terminal c, respectively in Fig. 5(b) for measurements in terminal d. Due to the symmetry, $XOR_c = XNOR_d$ and $XOR_d = XNOR_c$, at an energy of 0.21 meV being possible to implement all studied logice gates, except CNOT, for distinct values of α. The spin polarization values at E = 0.21 meV for the four posible input states in terminal c (black curve) and d (red curve) are illustrated in Fig. 6 as a function of the Rashba coefficient, the vertical lines indicating the α value for which the logic gates with the same line type as in Fig. 5 can be implemented in terminal c. As can be seen from Fig. 6, the spin polarizations have the following symmetries: $p_c^A(\alpha) = -p_d^D(-\alpha)$, $p_c^B(\alpha) = -p_d^B(-\alpha)$, $p_c^C(\alpha) = -p_d^C(-\alpha)$, $p_c^D(\alpha) = -p_d^A(-\alpha)$.

From Fig. 5 it follows that the CNOT gate cannot be implemented in a structure with a symmetric QPC. Therefore, we studied an asymmetric structure with $\Delta y_1 = 0$, $\Delta y_2 = 0.75L_y$, the rest of the parameters being the same. The corresponding results, presented in Fig. 7, show that in this case one can implement also the logic gate CNOT, at E = 0.14 meV being possible to implement all gates AND, OR, NOR and CNOT at different values of the Rashba coefficient/applied gate voltage. From Fig. 8, which illustrates the polarizations of the spin currents, it can be observed that in an asymmetric QPC only the symmetry relations

$p_c^A(\alpha) = -p_d^D(-\alpha)$ and $p_c^D(\alpha) = -p_d^A(-\alpha)$ hold, and the polarizations are maxima for α = 0.

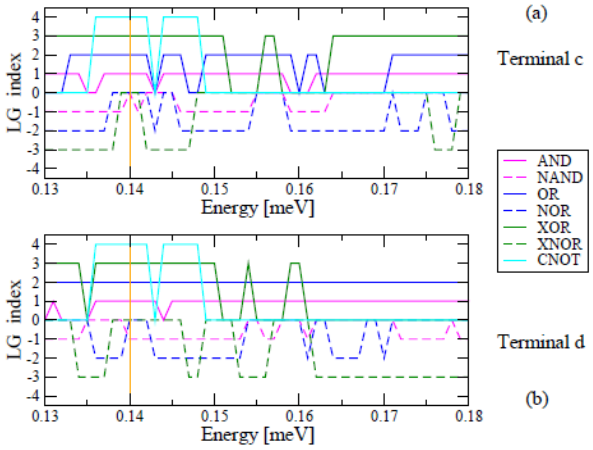


Fig. 7

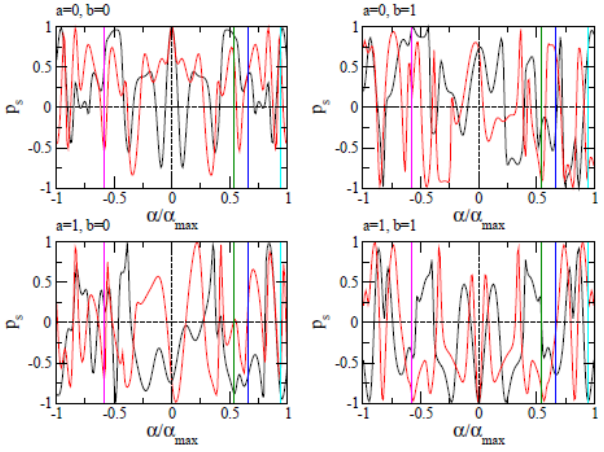


Fig. 8

These results, which show that the functionality of the configuration in Fig. 4 can be modified by varying a single parameter: α/gate voltage, so that several logic gates: AND/NAND, OR/NOR, XOR/XNOR and CNOT (for an asymmetric QPC) can be implemented, are being submitted to an ISI journal (vezi **A2**).

The second proposed configuration for implementing logice gates in a 2DEG with variable Rashba coefficients α_i in different regions subjected to different gate voltages, that can be independently controlled, is illustrated in Fig. 9. The advantage of this simple configuration is that the transport/transmission coefficient of ballistic electrons with energy E and effective mass m can be obtained analytically. More precisely, for a one-dimensional structure along x, with a Rashba Hamiltonian $H = p_x^2/2m - \alpha\sigma_y p_x/\hbar$, the wavefunction in each segment j, can be written as

$$\Psi_j = a_j \exp(ik_{+j}x)|\uparrow\rangle + b_j \exp(-ik_{-j}x)|\uparrow\rangle + c_j \exp(ik_{-j}x)|\downarrow\rangle + d_j \exp(-ik_{+j}x)|\downarrow\rangle \qquad (8)$$

where $|\uparrow\rangle$, $|\downarrow\rangle$ are the spin-up and spin-down eigenfunctions, and $k_{\pm j} = \pm k_{Rj} + \sqrt{k_{Rj}^2 + 2mE/\hbar^2}$, with $k_{Rj} = \alpha_j m/\hbar^2$. Applying at each interface the continuity condition for the wavefunction and that of current conservation, we obtain the following relation between the coefficients a, b, c, d at the input (layer 1) and output (layer 7) [9]:

$$\begin{pmatrix} a_1 \\ b_1 \\ c_1 \\ d_1 \end{pmatrix} = M \begin{pmatrix} a_7 \\ b_7 \\ c_7 \\ d_7 \end{pmatrix} = S_n^{-1} S_{R1} P_{R1}(L_1) S_{R1}^{-1} S_n P_n(D_1) S_n^{-1} S_{R2} P_{R2}(L_2)$$
$$\times S_{R2}^{-1} S_n P_n(D_2) S_n^{-1} S_{R3} P_{R3}(L_3) S_{R3}^{-1} S_n \begin{pmatrix} a_7 \\ b_7 \\ c_7 \\ d_7 \end{pmatrix} \qquad (9)$$

where

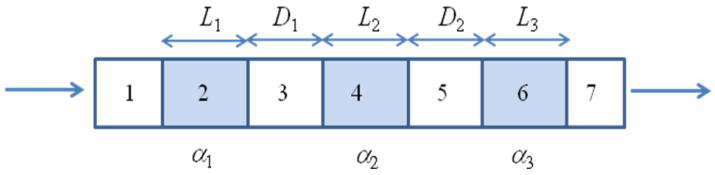


Fig. 9

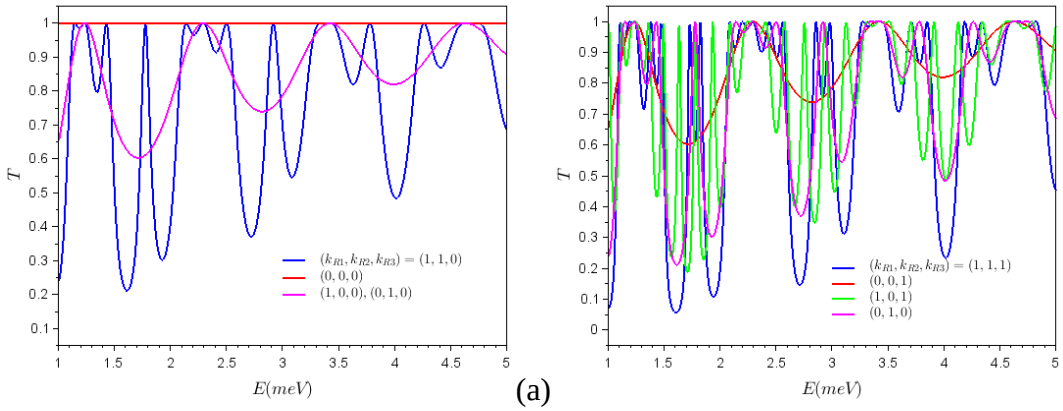
$$S_{Rj} = \begin{pmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ \hbar(k_{+j} - k_{Rj})/m & -\hbar(k_{-j} + k_{Rj})/m & 0 & 0 \\ 0 & 0 & \hbar(k_{-j} + k_{Rj})/m & -\hbar(k_{+j} - k_{Rj})/m \end{pmatrix},$$

$$P_{Rj}(L_j) = \begin{pmatrix} \exp(-ik_{+j}L_j) & 0 & 0 & 0 \\ 0 & \exp(ik_{-j}L_j) & 0 & 0 \\ 0 & 0 & \exp(-ik_{-j}L_j) & 0 \\ 0 & 0 & 0 & \exp(ik_{+j}L_j) \end{pmatrix},$$

$$S_n = S_{Rj}\big|_{k_{Rj}=0}, \quad P_n(D_j) = P_{Rj}(D_j)\big|_{k_{Rj}=0}$$

Then, the transmission coefficient of the spin-up wavefunction, for example, is $T = 1/|M_{11}|^2$, where M_{11} is the (1,1) element of the total matrix M.

To obtain as large as possible modulations of the transmission coefficient of ballistic electrons, we looked for systems with a large Rashba coefficient and a long mean free path. Such a system is the bidimensional interface $LaAlO_3/SrTiO_3$, in which quasi-onedimensional structures can be induced, and which has a mean free path of 20 μm at a temperature of 50 mK [10] and a giant Rashba coefficient, $k_R = 10^9$ m^{-1} [11]. The simulations in Fig. 10 correspond to $L_1 = L_2 = L_3 = D_1 = D_2 = 50$ nm, the input logic states being encoded in the Rashba coefficients values in the 3 regions, the 0 logic state being associated to $k_{Ri} = 10^4$ m^{-1}, $i = 1,2,3$ while the 1 value corresponds to $k_{Ri} = 8\times10^8$ m^{-1}. The output logic state is encoded in the transmission coefficient value. Thus, when the logic value of $k_{R3} = 0$ (see Fig. 10(a)), the studied configuration is equivalent with one with two inputs (a similar situation holds for $k_{R1} = 0$ or $k_{R2} = 0$, in the last case the distance between input states /gate electrodes being threefold) and implements the AND gate for inputs 1 and 2 (encoded in k_{R1} and k_{R2}) at energies for which T for (1,1,0) is much smaller than for (0,0,0), (1,0,0) and (0,1,0), for instance at $E = 1.6$ or 1.9 meV if the output logic state is 1 for $T < 0.5$ and zero otherwise, or at 2.7, 3.05 or 4 meV if the output logic state is 1 for $T < 0.6$ and zero otherwise; by identifying the output logic state with 1 for $T < 0.9$, at the same energies one can implement the OR gate. On the contrary, at $E = 1.8$ and 3 meV one can implement the logic gate CNOT with the control bit at the second input if $T < 0.85$ is associated with the logic value 1 and with 0 otherwise. If $k_{R2} = 0$ also, the configuration implements the NOT gate for input 1 at the energies 1.7, 2.9 or 4 meV if the output logic state is 0 for $T < 0.9$ and 1 otherwise. On the other hand, Figs. 10(a) and 10(b) suggest that a modified CCNOT gate (inverts the logic value of the target bit – at the input 3 – if the logic values of the other two bits are 0) can be implemented at $E = 4$ meV if the output is 0 for $0.6 < T < 0.9$.



(a) (b) Fig. 10

The original results regarding the functioning of a succesion of 3 regions with variable Rashba coefficients as logic gates are being finalized in order to be submitted for publication in a ISI journal (see **A3**).

Development of a correspondence between quantum spin and valley states for implementing new quantum computing configurations using valley states

Besides spin, the valley degree of freedom, although less studied, can implement logic gates with low power consumption. The advantage is that such logic gates are expected to have a longer coherence time, since the valley degree of freedom is more robust than spin at scattering/collisions due to a larger separation in the reciprocal space of the two unequivalent states. During activity 2.3 we realized a comparison/correspondenţce between the degrees of freedom of spin and valley with the aim of identifying/proposing logic gates based on valley states starting from logic circuit configurations based on spin qubits. In order to be relevant for this aim, such a correspondence cannot be limited to a formal identification of the two spin-up and spin-down states to the two unequivalent valley states, K and K', especially because the control of valley states is material-dependent, unlike the spin states that can be manipulated with a magnetic field, irrespective of the material. As such, the study regarding the excitation/detection modes of valley states, as well as of the manipulation mechanisms of this degree of freedom must be discussed separately with respect to the two types of materials in which the valley degree of freedom has been evidenced teoretically and/or experimentally: graphene (including bilayer graphene) and dichalcogenides. In this study we have taken into consideration only those characteristics that allow implementation of logic gates based on the interference/propagation of valley states in ballistic structures, and not on localized valley states (on potential wells, for example, as in [12]).

The vast majority of studies on valley states have concentrated up to now on their different excitation, in order to induce valley polarization and to mimic correspondic effects for spin states, such as Zeeman [13] or Hall [14].

Valley polarization can be achieved in principal by applying a uniaxial mechanic stress on a graphene sheet with mass/bandgap (grown on SiC or hBN substrates [15]), by using ferromagnetic electrodes in the case of dichalcogenides [16], or by optical excitation with an electromagnetic field polarized either circular [17] or elliptic [18]. Although in the case of optical excitation the valley polarization can be controlled, reaching values up to or over 90%, this method is difficult to be applied in integrated circuits.

Regarding dichalcogenides, or TMD (transition metal dichalcogenides), these are materials of type MX_2, where M is a transition metal (Mo, W, etc.) and X a chalcogenid (S, Se or Te). A

common characteristic of these materials, especially of atomic layers of these materials, is that the spin and valley states are coupled due to inversion symmetry breaking caused by their crystalline structure and the large spin-orbit coupling. This fact, and the fact that these materials have a mean free path/mobility significantly lower than in, limit the use of TMDs for implementing spin qubits.

On the other hand, in graphene sheets with a bandgap of width Δ in which the charge carriers with momentum $\boldsymbol{p}$ have an effective mass m, there is the valley-orbit interaction mechanism, described by the Hamiltonian

$$H_{vo} = \tau \frac{\hbar}{4m\Delta}(\boldsymbol{p} \times \nabla V) \cdot \hat{\boldsymbol{z}} \tag{10}$$

where τ is a valley index equal to -1 for K and +1 for K' and V is the potential energy. This Hamiltonian is in fact similar to that describing the Rashba spin-orbit coupling:

$$H_{so} = \frac{\alpha}{\hbar}(\boldsymbol{p} \times \boldsymbol{E} / |\boldsymbol{E}|) \cdot \boldsymbol{\sigma} \tag{11}$$

where $\boldsymbol{E}$ is the electric field and α is the Rashba coefficient. Although the valley-orbit interaction has a greater tunability potential in bilayer graphene than in monolayer graphene, a gate voltage in the first case allowing the independent control of both Fermi level and bandgap width [19], even in monolayer graphene this interaction mechanism induces valley polarization via an electric field applied by a side gate [20]. In addition, in monolayer graphene the two valley states are mixed in a proportion of 50:50 in an armchair nanoribbon, the resulting state being suitable to be used as starting state in quantum algorithms, being equivalent to that obtained by applying a Hadamard gate.

As result of activity Act. 2.3 we reached the following conclusions necessary to finalize Act. 2.4 in 2019, according to the Realization plan of the project:

- as material for logic gates involving valley states, the most suitable from the point of view of mean free path and the possibility of manipulating these states is bilayer graphene, although it is not clear up to now if armchair nanoribbons from this material can be used as starting states for quantum algorithm implementation;

- as manipulation mechanism of valley states, the most suitable for implementing interference/ propagation based logic gates is the valley-orbit interaction – mechanism specific to graphene, including bilayer graphene, which can be controlled by gate voltages;

- as excitartion/detection mechanism of valley states, we identified the most suitable one as being that using armchair nanoribbons in conjunction with Bell-state measurements/spatial separation of different valley states

- as promissing configurations for logic gates, we will concentrate on similar ones to those reported here involving spin states in the presence of the Rashba effect

Preliminary results regarding the development of plasmonic logic gate configurations using slot waveguides

Although the design of plasmonic logic gate configurations on slab waveguides is expected to be studied in the 2019 stage of the project, we have considered necessary to start investigating this subject earlier due to its complexity. More precisely, we have performed a preliminary identification of possible configurations of interest and modeled them with a simple method

based on the analogy with transmission lines. In 2019 we intend to improve the simulation method using performant computing algorithms and to optimize them in order to fabricate such logic circuits based on plasmonic slot waveguides.

We have identified two configurations of plasmonic logic gates of interest. The first one refers to reconfigurable logic gates, potentially interesting, but quite difficult to realize experimentally since not only the fabrication of slot waveguides must be controlled strictly but also the realization of the regions with a variable refractive index (graphene or liquid crystals). The second configuration is based on ring-shaped plasmonic waveguides, with several input/output ports, less technologically demanding, but the simulation of which should be improved to take into account the influence of the curvature on plasmon propagation. We detail these configurations in the following.

Reconfigurable plasmonic logic gates

The proposed configuration consists of a slot plasmonic waveguide, of width W, formed from a dielectric medium (air) with permittivity ε_a, surrounded by metal (for example, silver), with permittivity ε_{Ag}. Along this waveguide there are several regions, with lengths L_i, (i = 1, 2 and 3 in Fig. 11(a)), with permittivities ε_{gr} that can be controlled by applied voltages.

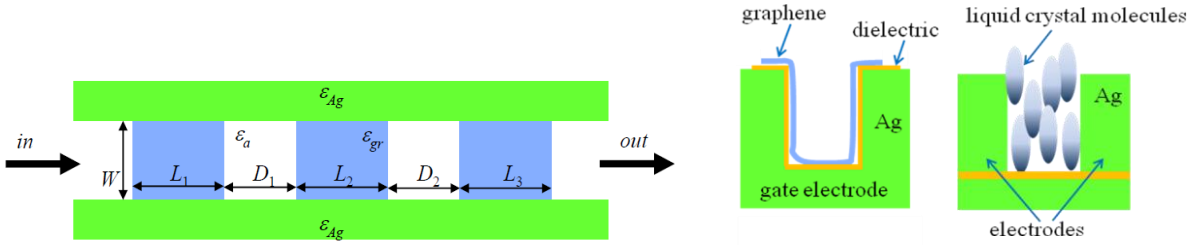


Fig. 11 (a) (b)

As suggested in Fig. 11(b), these regions can be covered by a graphene sheet, the permittivity of which can be modified by a gate voltage applied directly on the metal, or by liquid crystals, the permittivity of which varies with the bias applied on the two parts of the waveguide, which should be isolated. For a graphene-covered waveguide, in which the permittivity can be varied in wide ranges [21], we denote by $\varepsilon_{gr} = \varepsilon_0$ and $\varepsilon_{gr} = \varepsilon_1$ the permittivities corresponding to the logic states 0 and, respectively, 1, the associated gate voltages being V_0 and V_1.

This configuration can implement plasmonic logic gates with one, two or three bits by encoding the input logic states in the tunable permittivity/gate voltage values applied on the covered regions, minimizing thus the problems with plasmon excitation. The values of the transmission coefficient/transmitance T encode the output logic state. This circuit is based on modulating the light interference via varying the permittivity of the covered regions, and can be modeled with the help of the analogy with transmission lines [22-24], which holds in slot waveguides that support only one propagating mode. For an operating wavelength of 1.55 μm, this restriction imposes that W = 40 nm.

To illustrate how this circuit works, we consider first the implementation of the logic gate NOT, for which only one region with variable permittivity is needed. The dependence of the transmitance T on wavelength in this case is shown in Fig. 12(a) for L_1 = 355 nm, the solid and dashed curves correspunding to ε_0 = 1.2 and ε_1 = 5. From this figure it follows that, at λ = 1.55 μm, T can have high values, associated to the output logic state/value of 0, for instance, or small values, coded as logic state 1. The NOT gate can be implemented by varying the gate voltage from V_0 to V_1.

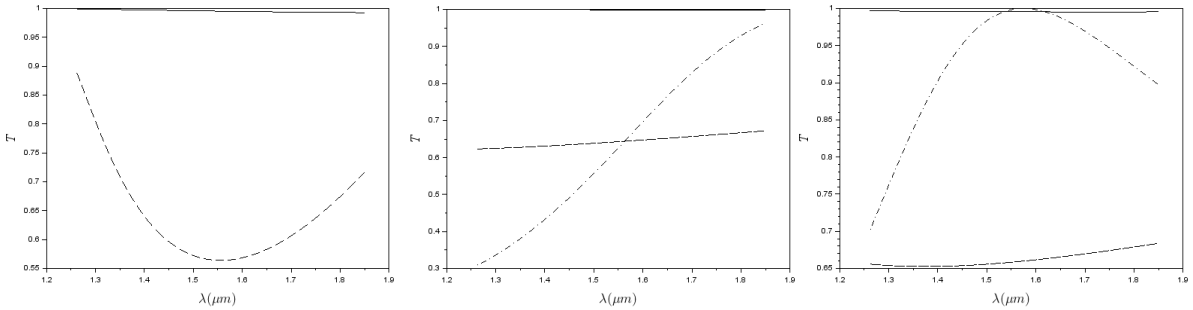
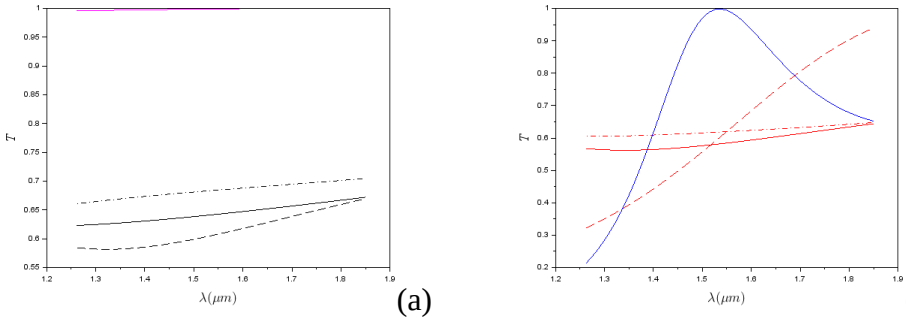


Fig. 12 (a) (b) (c)

If the slot waveguide is covered with two graphene sheets of lengths L_1 and L_2, separated by a distance D_1, that can be controlled independently by gate voltages, one can implement logic operations involving two bits. In the example in Fig. 12(b), in which $L_1 = L_2 = D_1 = 100$ nm, $\varepsilon_0 = 1.2$ and $\varepsilon_1 = 4.75$, the spectral dependence of the transmission was plotted for the input states 00 (solied line), 01 (dashed line), 10 (dotted line) and 11 (dashed-dotted line); the notation for the input states, XY ($X = 0,1$, $Y = 0,1$), shows that the voltage applied on the first graphene region is V_X and on the second one is V_Y. From Fig. 12(b), in which the curves for 01 and 10 overlap, and the curve for 00 has T almost equal to 1 on the whole spectral range, it can be observed that at 1.55 μm the transmitance is either close to 1 (high) or 0.65 (low). If large values of T are associated to the logic value 0 and small values to 1, the proposed configuration implements the OR gate, while an opposite association of both input logic states (1 for permittivity ε_0/voltage V_0 and 0 for ε_1/V_1) and output logic states (1 for T high, 0 for T low) allows the implementation with the same waveguide of the logic gate AND.

The same configuration with two regions covered with graphene, but for $L_1 = L_2 = 100$ nm, $D_1 = 45$ nm, $\varepsilon_0 = 1.2$ and $\varepsilon_1 = 4.5$ can implement the reversible CNOT gate at 1.55 μm if the input states 0 and 1 correspond to V_0 and, respectively, V_1, as can be seen from Fig. 12(c) illustrating the spectral dependence of T for the input states 00, 01, 10 and 11 with the same line type as in the example above; again, the curves for 01 and 10 overlap. However, in this case the output logic state 0 is identified with a large value for T and the 1 state with a low T value, the target bit being the first bit and the control bit the second one.



(a) (b) Fig. 13

When there are three graphene sheets, the permittivity of which can be independently controlled, one can implement logice gates implying three bits. For instance, to implement the universal and reversible Toffoli gate, which changes the logic value of one/target bit if two control bits are 1, we can identify the target bit as the first bit/graphene region, with logic states 0 and 1 coded in ε_{0t} and ε_{1t}, and the control bits with the other covered regions, the logic states 0 and 1 of which are coded in the permittivity values ε_{0c} and ε_{1c}. Figures 13(a) and 13(b) illustrate, respectively, the spectral dependence of the transmitance when the target bit is 0 and $\varepsilon_{0c} = 4.75$, $\varepsilon_{1c} = 1.2$, and, respectively, when it has the value of 1 and $\varepsilon_{0c} = 1.2$, $\varepsilon_{1c} =$

4.75, for $L_1 = L_2 = L_3 = D_1 = D_2 = 100$ nm, $\varepsilon_{0t} = 1.2$ and $\varepsilon_{1t} = 5$. The continuous, dashed and dashed-dotted black curves in Fig. 13(a) correspond to the states of th three graphene-covered regions (in order) 000, 010 and 001, and the magenta curve corresponds to the state 011. Similarly, the continuous, dashed and dashed-dotted red curves in Fig. 13(b) correspond to the input states 100, 110 and 101, and the blue curve to 111. These dependences, which indicate a change in the transmitance from small to large values around $\lambda = 1.55$ μm when both control bits are 1, correspond to the Toffoli gate if we define the output logic state as 0 when T is small (< 0.7) and 1 when T is large (> 0.95) in Figs. 13(a) and oppositely in Fig. 13(b)).

The results regarding the simulation of this reconfigurable plasmonic configuration with one, two or three covered regions (actually, with three regions, each of which equivalent to air if the relative permittivity is tuned to 1) was accepted an an ISI journal (see **A4**)

Ring-shaped logic circuits, with multiple input/output ports

This configuration is compact, versatile, and can be easily combined in cascade to implement complex computing algorithms, the output logic states, encoded in the transmittance value in one port, depending on the geometry and the phase of incident electromagnetic fields in all other ports. In particular, we have studied configurations with 3 (see Fig. 14(a)) and 4 ports, concluding that, once the number of ports increases the complexity of the response increases also and, respectively, the fabrication tolerances become stricter. Therefore, it is preferable to arrange in cascade two 3-port circuits, as in Fig. 14(b), than to use configurations with a larger number of ports. As in the previous configuration, the propagation of electromagnetic fields in multi-port ring-shaped plasmonic waveguides was simulated using the analogy with the transmission modes, method that can be applied if only one propagating mode exists. In addition, we have chosen symmetric configurations to take advantage of the even-odd mode analysis method in transmission line circuits. In all cases the width of the Ag/aer/Ag slot waveguide is $d = 50$ nm and the excitation wavelength is $\lambda = 550$ nm.

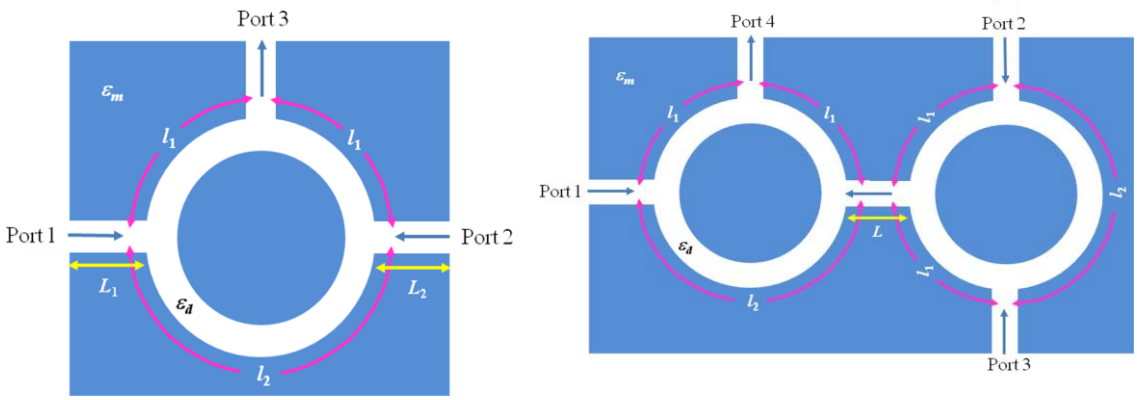


Fig. 14 (a) (b)

For example, in a symmetric structure, as in Fig. 14(a), for which $l_2 = 2l_1$ (lengths measured between the centers of the input/output waveguides), the output intensity $T = |t|^2$, with amplitude t, is represented in Fig. 15 as a function of l_1, the complex input signals at ports 1 and 2 being denoted as a_1 and $a_2 \exp\phi$, with a_1, a_2 the signal amplitudes and ϕ their relative phase. From this figure, which shows the results for $a_1 = 1$, $a_2 = 1$, $\phi = 0$; $a_1 = 1$, $a_2 = 0$ or $a_1 = 0$, $a_2 = 1$, irrespectiv of ϕ; and $a_1 = 1$, $a_2 = 1$, $\phi = \pi$ or $a_1 = 0$, $a_2 = 0$ (see the legend), it follows that T is periodic in l_1/the output intensity is maximum if $l_1 k_{SPP}$ is an integer

multiple of π, and this maximum T value is 4 times larger than the value corresponding to the case when only one input is present.

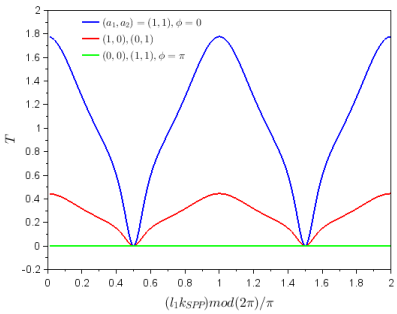


Fig. 15

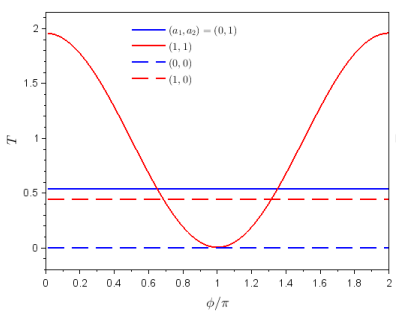


Fig. 16

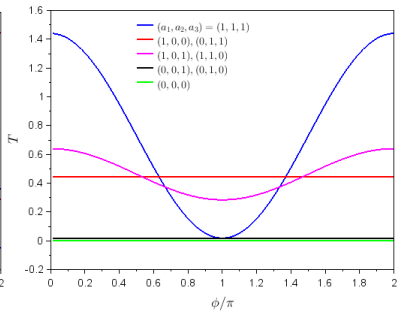


Fig. 17

For T maxim, codând stările logice de intrare 0 and 1 în valorile 0 and 1, respectiv 0 and 1.2, ale amplitudinilor la porturile 1 and 2 [25], se observă din Fig. 16 că circuitul cu 3 porturi implementează poarta ireversibilă OR for $\phi = 0$ (intrări în fază) if starea logică de la ieandre este identificată ca 1 for $T > 0.3$ and 0 în caz contrar. În Fig. 16 (vezi legenda) sunt reprezentate curbele corespunzătoare intrărilor $(a_1,\ a_2) = (0,1)$, (1,1), (0,0) and (1,0). În mod analog, for $\phi = \pi$ (intrări în anti-fază), circuitul poate implementa poarta ireversibilă XOR for acelaand mod de definire a stării de ieandre, adică ieandrea este 1 doar if $(a_1,a_2) = (0,1)$ sau (1,0). Pe de altă parte, if în Fig. 15 starea logică de ieandre 1 corespunde la $T > 1$ and este 0 în caz contrar, circuitul implementează poarta ireversibilă AND if intrările sunt în fază, adică valoarea la ieandre este 1 doar if $(a_1,a_2) = (1,1)$.

Circuitul cu 3 porturi poate implementa and poarta reversibilă CNOT gate, care inversează valuarea logică a unui qubit if bitul de control este 1 and îl lasă neschimbat în caz contrar. More precisely, as shown in Fig. 16, for the control bit at port 2 and the target bit at port 1, the circuit implements the CNOT gate if ϕ takes values between 0.7π and 1.3π (for instance, $\phi = \pi$) and if the output bit is 1 for $T > 0.3$. In particular, if there is qubit/logic state 1 at port 2, the configuration implements the NOT gate for the input at port 1 in the same conditions as above. Analogously, one can find/define output states in a 4-port configuration as a function of its dimensions, and the amplitudes and phases of the input signals.

To illustrate how a cascaded configuration of two 3-port ring waveguides, as in Fig. 14(b), can implement the CCNOT gate, we consider two circuits with $l_1 k_{SPP}$ an integer multiple of π and $l_2 = 2l_1$, in which the logic values 1 of the input states (a_1,a_2,a_3) are encoded in the amplitude values $a_1 = 1,\ a_2 = a_3 = 0.4$, and have the logic value 0 if there is no signal at the respective port. The dependence of the output intensity at port 4 on the phase diference ϕ between the inputs at the left circuit (port 1 and the output – port 3 of the right circuit)/length L is represented in Fig. 17 for in-phase inputs at ports 2 and 3 for $(a_1,a_2,a_3) = (1,1,1)$ (blue line), (1,0,0) or (0,1,1) (red line), (1,0,1) or (1,1,0) (magenta), (0,0,1) or (0,1,0) (black line) and (0,0,0) (green). Figure 17 demonstrates that the circuit consisting of two cascaded ring waveguides can implement the CCNOT gate for the target bit at port 1 if the other bits/inputs are control bits and if the output intensity has the logic state 1 for $T > 0.2$ for ϕ in the interval $0.75\pi - 1.2\pi$.

The results obtained regarding the modeling of multi-port slot waveguides circuits were acceptate spre publicare într-o revistă ISI (vezi **A5**), and au fost diseminate la o conferinţă internaţională (vezi **C3**).

In parallel with modeling possible logic plasmonic configurations, we have obtained some preliminary results on the fabrication of some slot waveguides, which we have disseminated at two international conferences (**C4** and **C5**)

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Accepted/submitted/to be submitted articles in ISI journals in 2018

A1: A. Radu, S. Iftimie, D. Dragoman – Ballistic 3-port interferometric logic gates in the quantum Hall regime, submitted to Physica E

A2: G.A. Nemnes, D. Dragoman – Reconfigurable quantum logic gates using Rashba controlled spin polarized currents, submitted to Physica E

A3: S. Iftimie, A. Radu, D. Dragoman – Reconfigurable quantum logic gates with gate-controlled Rashba spin-orbit coupling, in final redactation stage for submission to Journal of Applied Physics

A4: E. Vladescu, D. Dragoman – Reconfigurable plasmonic logic gates, Plasmonics, online https://doi.org/10.1007/s11468-018-0737-z

A5: D. Dragoman, E. Vladescu – Ring-shaped plasmonic logic gates, Plasmonics, online https://doi.org/10.1007/s11468-018-0779-2

Contributions at international conferences in 2018 (the first two contributions disseminated results obtained in 2017)

C1: G. A. Nemnes, T. L. Mitran, D. Dragoman - Electric field control in ballistic graphene Y-junctions, TIM 18 Physics Conf, 24-26 May 2018, Timişoara, România

C2: G. A. Nemnes, T. L. Mitran, D. Dragoman - Ballistic transport in graphene Y-junctions, 18th International Balkan Workshop on Applied Physics and Materials Science (IBWAP 2018), 10-13, July, 2018, Constanţa, România

C3: D. Dragoman, E. Vladescu - Multiport ring-shaped plasmonic waveguides operating as logic gates, 18th International Balkan Workshop on Applied Physics and Materials Science (IBWAP 2018), 10-13, July, 2018, Constanţa, România

C4: V.-A. Antohe, S. Iftimie, A. Radu, L. Ion, D. Dragoman - On the fabrication and characterization of slot waveguides on silicon and aluminum, 18th International Balkan Workshop on Applied Physics and Materials Science (IBWAP 2018), 10-13, July, 2018, Constanţa, România

C5: S. Iftimie, A. Radu, V.-A. Antohe, L. Ion, D. Dragoman - Fabrication and characterization of slot waveguides for plasmonic logic gates, 12th International Conf. on Physics of Advanced Materials, 22-28 Sept. 2018, Heraklion, Greece

Project Director,

Prof. dr. Daniela Dragoman